

In The Claims:

Please amend the claims as follows:

1. (Original) A method for fabricating a non-volatile memory device, comprising the steps of:

forming a gate pattern in which a first conductive layer is used as a floating gate, a second conductive layer is used as a control gate, the first conductive layer, a dielectric layer, and the second conductive layer are sequentially stacked on a semiconductor substrate;

forming a polishing stopper on the gate pattern and the semiconductor substrate;

forming an interlayer insulating layer on the polishing stopper;

forming a common source line (CSL) by etching a portion of the interlayer insulating layer, and a portion of the polishing stopper, and depositing a conductive material to the etched portions;

planarizing the common source line and the interlayer insulating layer until the surface of the polishing stopper is exposed;

partially etching back the polishing stopper until the surface of the second conductive layer is exposed; and

forming a silicide layer on the exposed second conductive layer and the common source line.

2. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein an oxide layer is formed on the semiconductor substrate.

3. (Currently Amended) The method for fabricating a non-volatile memory device of claim 2, wherein the oxide layer is formed to a thickness of about 50 angstrom to about 200 angstrom.

4. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the first conductive layer and the second conductive layer is a doped polysilicon layer.

5. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the dielectric layer is a multi-layer comprising an oxide layer and a nitride layer.

6. (Currently Amended) The method for fabricating a non-volatile memory device of claim 1, wherein the dielectric layer is formed to a thickness of about 100 angstrom to about 200 angstrom.

7. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the gate pattern further comprises an insulating layer additionally formed on the second conductive layer.

8. (Original) The method for fabricating a non-volatile memory device of claim 7, wherein the insulating layer is formed with one of a mono-layer nitride layer and a multi-layer containing a nitride layer.

9. (Original) The method for fabricating a non-volatile memory device of claim 1, further including the step of forming spacers on side walls of the gate pattern.

10. (Original) The method for fabricating a non-volatile memory device of claim 9, wherein the spacers are formed with one of a mono-layer nitride layer and a multi-layer containing a nitride layer.

11. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the polishing stopper is made of a nitride layer.

12. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the interlayer insulating layer is an oxide layer or a multi-layer including an oxide layer.

13. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the conductive material for forming the common source line is made of polysilicon containing impurities.

14. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the step of etching back the polishing stopper is performed by a wet etching method using phosphoric acid.

15. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the step of etching back the polishing stopper is performed by a dry etching method.

16. (Currently Amended) The method for fabricating a non-volatile memory device of claim 1, wherein the silicide layer is a silicide selected from the silicide group consisting of cobalt silicide (CoSix), tungsten silicide (~~Wsix~~ WSix) and aluminum silicide (AlSix).

17. (Original) The method for fabricating a non-volatile memory device of claim 1, wherein the non-volatile memory device is a NAND type flash memory.

18. (Original) A semiconductor non-volatile memory device formed by process steps comprising:

forming a gate pattern on a semiconductor substrate, the gate pattern having first and second conductive layers and a dielectric layer therebetween;
forming a polishing stopper on the gate pattern and the semiconductor substrate;
forming an interlayer insulating layer on the polishing stopper;

forming a common source line (CSL) by etching a portion of the interlayer insulating layer, and a portion of the polishing stopper, and depositing a conductive material;

then, planarizing the common source line and the interlayer insulating layer until the surface of the polishing stopper is exposed;

partially etching back the polishing stopper until the surface of the second conductive layer is exposed; and

forming a silicide layer on the exposed second conductive layer and the common source line.

19. (New) The device of claim 18, further including an additional insulating layer on the second conductive layer.

20. (New) The device of claim 18, wherein the non-volatile memory device is a NAND type flash memory.